Old Company Name in Catalogs and Other Documents

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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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NP109N055PUJ

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP109N055PUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
NP109N055PUJ-E1B-AY Note		Tape 1000 p/reel		
NP109N055PUJ-E2B-AY Note	Pure Sn (Tin)		TO-263 (MP-25ZP) typ. 1.5 g	

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

Super low on-state resistance
 R_{DS(on)} = 3.2 mΩ MAX. (V_{GS} = 10 V, I_D = 55 A)

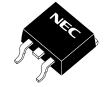
(TO-263)

Low input capacitance
 C_{iss} = 6900 pF TYP.

• Designed for automotive application and AEC-Q101 qualified

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	VDSS	55	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±110	Α
Drain Current (pulse) Note1	I _{D(pulse)}	±440	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	220	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Energy Note2	Eas	291	mJ
Repetitive Avalanche Current Note3	IAR	54	Α
Repetitive Avalanche Energy Note3	Ear	291	mJ



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 28 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

3. Tch \leq 150°C, Rg = 25 Ω

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	0.68	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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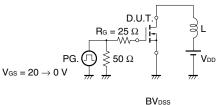
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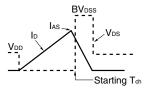
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 55 V, V _{GS} = 0 V			1	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 5 V, I _D = 55 A	45	101		S
Drain to Source On-state Resistance Note	R _{DS(on)}	V _{GS} = 10 V, I _D = 55 A		2.5	3.2	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V,		6900	10350	pF
Output Capacitance	Coss	V _{GS} = 0 V,		760	1140	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		290	530	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 28 V, I _D = 55 A,		40	90	ns
Rise Time	tr	V _G S = 10 V,		20	50	ns
Turn-off Delay Time	t _{d(off)}	$R_G = 0 \Omega$		90	180	ns
Fall Time	tf			10	30	ns
Total Gate Charge	Q _G	V _{DD} = 44 V,		115	180	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V,		26		nC
Gate to Drain Charge	Q _{GD}	I _D = 110 A		38		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 110 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	I _F = 110 A, V _{GS} = 0 V,		57		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>μ</i> s		115		nC

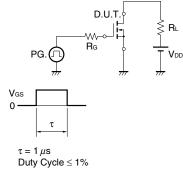
Note Pulsed test

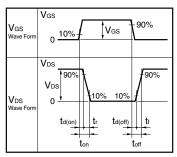
TEST CIRCUIT 1 AVALANCHE CAPABILITY





TEST CIRCUIT 2 SWITCHING TIME

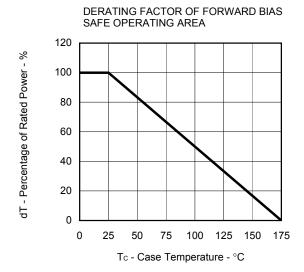


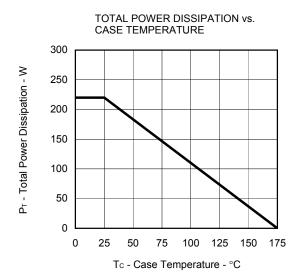


TEST CIRCUIT 3 GATE CHARGE

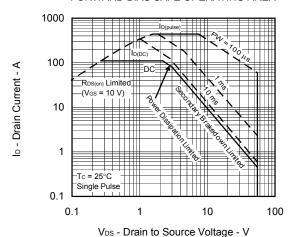
$$\begin{array}{c|c} \text{D.U.T.} & \\ \text{Ig} = 2 \text{ mA} & \text{Im} \\ \hline \\ \text{PG.} & \\ \end{array} \begin{array}{c} \text{S} \text{50 } \Omega \\ \end{array} \begin{array}{c} \text{V}_{\text{DD}} \\ \end{array}$$

TYPICAL CHARACTERISTICS (TA = 25°C)

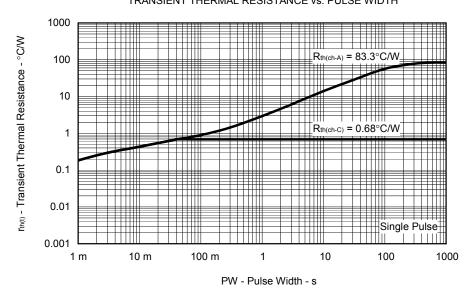




FORWARD BIAS SAFE OPERATING AREA

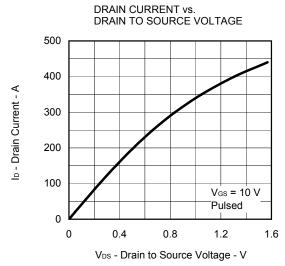


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

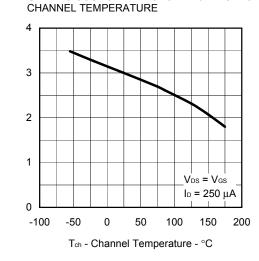


Data Sheet D19729EJ1V0DS

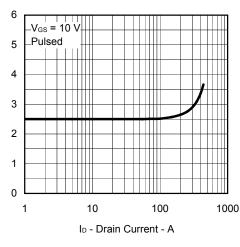
Vos(th) - Gate to Source Threshold Voltage - V



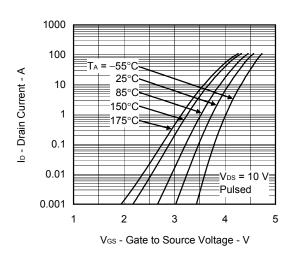




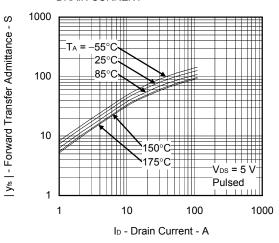
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



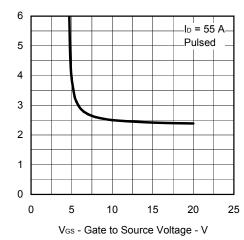
FORWARD TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

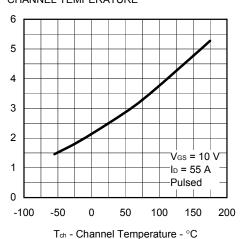


R_{DS(on)} - Drain to Source On-state Resistance - mΩ

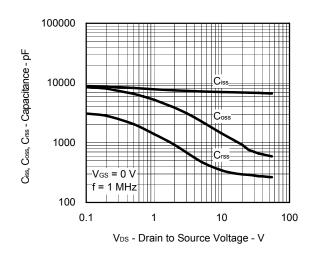
RDS(on) - Drain to Source On-state Resistance - mΩ

$\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

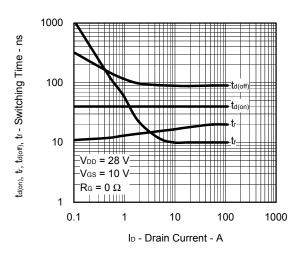
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



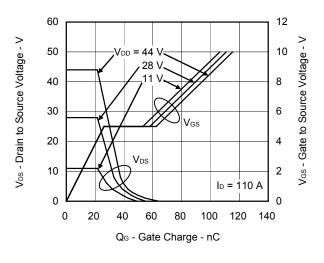
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



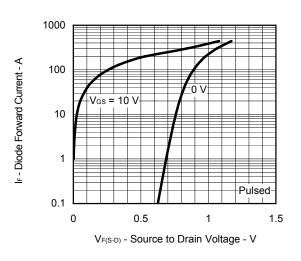
SWITCHING CHARACTERISTICS



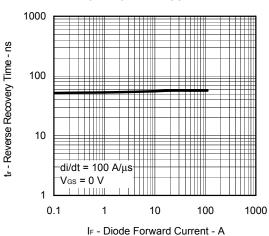
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

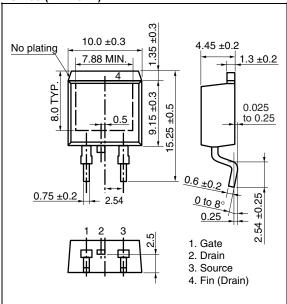


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

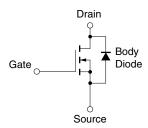


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



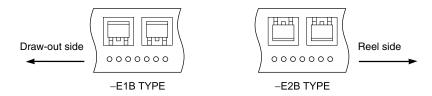
EQUIVALENT CIRCUIT



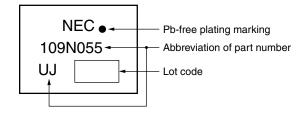
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

TAPE INFORMATION

There are two types (-E1B, -E2B) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP109N055PUJ should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below	IR60-00-3
	Time at maximum temperature: 10 seconds or less	
	Time of temperature higher than 220°C: 60 seconds or less	
	Preheating time at 160 to 180°C: 60 to 120 seconds	
	Maximum number of reflow processes: 3 times	
	Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	
Partial heating	Maximum temperature (Pin temperature): 350°C or below	P350
	Time (per side of the device): 3 seconds or less	
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	

Caution Do not use different soldering methods together (except for partial heating).

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